RESEARCH GROUP PROFILE

Computer Architecture and Technology Group

1.- Contact details

Contact Person	
Title	Juan Antonio
First Name	Maestro de la Cuerda
Family Name	C/ Pirineos 55, 28040 Madrid, España
Address	Int+34914521100
Telephone	Int+34914521110
Fax	jmaestro@nebrija.es
e-mail	http://www.nebrija.es/~jmaestro/esa/researchPapers.htm

2.- Work Team

First and Family Name	Title	Principal Function / Activity
Juan Antonio Maestro	PhD. (UCM)	Director
Pedro Reviriego	PhD. (UPM)	Co-director
Oscar Ruano	MSc.	Phd. Student
Shih-Fu Liu	MSc.	Phd. Student

3.- Description of the Group Expertise

Activity	Description
Electronic designs for space applications	Development of fault tolerant circuitos for space applications. Verification and testing through software based fault injection. Collaborations with ESA, INAF-Milán, Univerity College Dublin, Alter-group,etc.
Memory Reliability and fault tolerance	Development of memory reliability estimation models and MBUs and MCUs mitigation techniques. Study of error correction codes (ECC) for memories. Collaborations with Cisco, Hanyang University, Oxford Brookes University, etc.
Computer network energy efficiency	Development of low power consumption techniques for Ethernet Networks based on Energy Efficient Ethernet standard (802.3az). Collaborations with Lawrence Berkeley Laboratory, University of South Florida, Universidad Carlos III, etc.

4.- Keywords describing the expertise showed

Activity	Keywords
Electronic designs for space applications	**1.- Space** **2.- Radiation on Integrated Circuits** **3.- Fault tolerant Digital Circuits** **4.- Optimized TMR** **5.- Digital Circuits** **6.- System availability** **7.- Single Event Upset (SEU)**
Memory Reliability and fault tolerance	**1.- SRAM memories** **2.- Soft error** **3.- Interleaving** **4.- Mean Time to Failure** **5.- Memory Models** **6.- Multiple Cell Upsets (MCUs)** **7.- Error Correction Codes (ECC)**
Computer network energy efficiency	**1.- Energy Efficiency** **2.- Ethernet** **3.- IEEE 802.3**

5.- National and/or International R+D Projects involved

Project Title	Programme	Start and end dates of project
Diseño, simulación y experimentación con radiación sobre memorias y otros circuitos digitales complejos para aplicaciones espaciales embarcadas.	**AYA2009-13300-C03** **Ministerio de Educación y Ciencia de España.**	**Jan. 2010/Jan. 2013**
Brief descripction (max. 500 characters)	**Study of radiation effects on SRAM memories and improvement of existing fault tolerant techniques in terms of area, power consumption etc.**	
Activities performed	**Feed Forward Equalizer protection techniques.** **Proposal of MBUs prediction models for memories.** **Proposal of optimized selective TMR based on topological circuit analysis.**	

Project Title	Programme	Start and end dates of project
FT-GALILEO: Análisis de un transceptor GALILEO y propuesta de técnicas de optimización para su diseño eficiente y tolerante a fallos.	**30/2009 Aeroespacial,** **Comunidad Autónoma de Madrid.**	**Jan. 2009/Jun. 2010**
Brief descripction (max. 500 characters)	**Radiation effect Studies of the Galileo transceiver and proposal of fault tolerant techniques for mitigating malfunction in space.**	
Activities performed	**Review of the Galileo FFT module.** **Proposal of fault tolerant technique for FFT** **Collaboration with INAF for measuring the quality of the proposed technique with FLIPPER** **General protection techniques for FSMs based on duality and one-hot code.** **Development of smart Engine for identifying SEU sensitive part of the system.**	

Project Title	Programme	Start and end dates of project
Estudio de Técnicas de Protección frente a los efectos de la Radiación en entornos Espaciales para Circuitos Digitales de Procesado de Señal.	**ESP2006-04163,** **Ministerio de Educación y Ciencia de España.**	**Oct. 2006/Oct. 2009**
Brief descripction (max. 500 characters)	**Space Radiation effect studies of moving-average filters widely used in telecommunication systems.**	
Activities performed	**Analysis and maintenance of the SST fault injection tool (ESA).**	

	Study of moving-average filter. **Proposal of improve fault tolerant techniques in terms of area cost compared to traditional methods like TMR and Hamming.**	
Project Title	**Programme**	**Start and end dates of project**
RadEsSim - Estudio de la Radiación en el Espacio: Simulación de los Efectos en Circuitos Digitales y Diseño de Implementaciones Tolerantes a Fallos.	**1/2007 Aeroespacial,** **Comunidad Autónoma de Madrid.**	**Jan. 2007/Apr. 2009**
Brief descripction (max. 500 characters)	**Simulation of radiation effect on ICs based on software injection and comparison between proposed techniques and standard TMR.**	
Activities performed	**Upgrading and updating of the SST injection tool.** **Development of the software fault injection platform for VHDL models.** **Proposal of SEU fault protection techniques.** **Discussion and analysis of the final results in comparison to classic methods.**	
Project Title	**Programme**	**Start and end dates of project**
EMULASER – Emulación mediante irradiación láser de los efectos de la radiación cósmica en componentes electrónicos.	**PNE-034/2006,** **Ministerio de Industria, Turismo y Comercio de España.**	**Oct. 2006/Dec. 2008**
Brief descripction (max. 500 characters)	**Study of laser source parameters required for simulation of radiation effects on ICs.** **Development of fault injection system in order to reduce the test cost of systems and protection techniques.**	
Activities performed	**Help and support for the development of laser injection model.** **Verification of the laser injection model through simulated injection techniques.**	

6.- National and/or International Organizations / Associations (Research Group or its members)

Organization	Country	Principal Activity
IEEE		Advancing technological innovation

7.- Brief Profile of the team work (max. 7-8 lines for each)

First and Family Name	Brief C.V.
Juan Antonio Maestro	Holds a M.Sc. degree in Physics (1994) and a Ph.D. degree in Computer Science (1999) from Universidad Complutense de Madrid. He has served both as a lecturer and researcher at several universities, as Universidad Complutense de Madrid, UNED (Open University), Saint Louis University and Universidad Antonio de Nebrija, where he currently manages the Computer Architecture and Technology Group. His current activities are oriented to the Space field, with several projects on reliability and radiation protection, as well as collaborations with the European Space Agency. He is the author of numerous technical publications, both in journals and international conferences. Besides from this, he has worked for several multinational companies, managing IT projects as a PMP, and organizing support departments. His areas of interest include High Level Synthesis and co-Synthesis, Signal Processing and Real-Time systems, Fault-tolerance and Reliability. jmaestro @ nebrija.es
Pedro Reviriego	Received the M.Sc. and Ph.D. degrees (Honors) from Technical University of Madrid in 1994 and 1997, both in Telecommunications Engineering. From 1997 to 2000 he was an R&D engineer at Teldat working on router implementation. In 2000 he joined Massana to work on the development of 1000BaseT transceivers. During 2003 he was a Visiting professor at University Carlos III. From 2004 to 2007 he was Distinguished Member of Technical Staff with LSI Corporation working on the development of Ethernet transceivers. He is currently with Universidad Antonio de Nebrija. His research interests are fault tolerant systems, performance evaluation of communication networks and the design of physical layer communication devices. He has authored numerous papers in international conferences and journals. He has also participated in the IEEE 802.3 standardization for 10GBaseT. previrie @ nebrija.es
Oscar Ruano	Holds a M.Sc. in Computer Engineering (2005) from Universidad Antonio de Nebrija. He has worked with different multinational companies in the IT consultancy field, as Accenture. Currently, he is a full-time researcher at Universidad Antonio de Nebrija, as well as a Ph.D. candidate.

	oruano @ nebrija.es
Shih-Fu Liu	**Received the B.Sc. in Electronic Engineering from Carinthian Tech Institute in Austria and the M.Sc. in Computer System Engineering from Technical University of Denmark in 2003 and 2005, respectively. He has worked in cooperation with multinational companies and various universities all over Europe in the European project SoC-Mobinet (IST-2000-30094) developing a design and FPGA-implementation of a run-time re-programmable high performance multi-rate filter processor. Currently, he is a full-time researcher at Universidad Antonio de Nebrija, as well as a Ph.D. candidate.** **sliu @ nebrija.es**